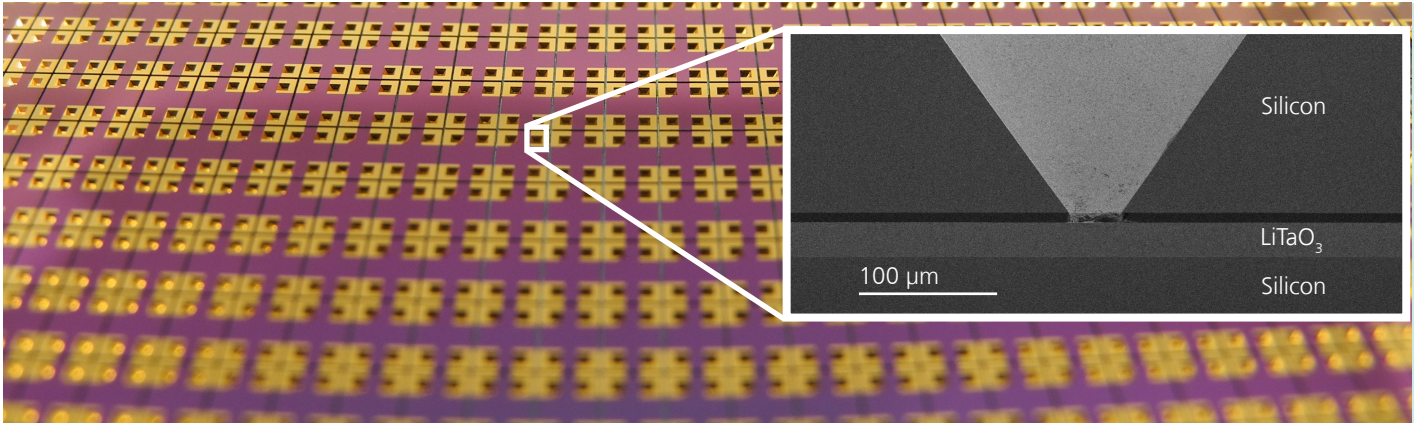


# SEMI-FINISHED BONDED SUBSTRATES



## Contact

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## Description

Semi-finished bonded substrates play a decisive role of low-cost and economic MEMS production. They are usually designed to correspond in form and dimensions of the produced MEMS product. The material and surface qualities are often optimized for specific applications and manufacturing processes.

As basic substrate for MEMS applications Fraunhofer ENAS offers bonded and structured (e.g. cavities, channels, through holes) wafers.

These stacks can be bonded using different wafer bonding technologies like:

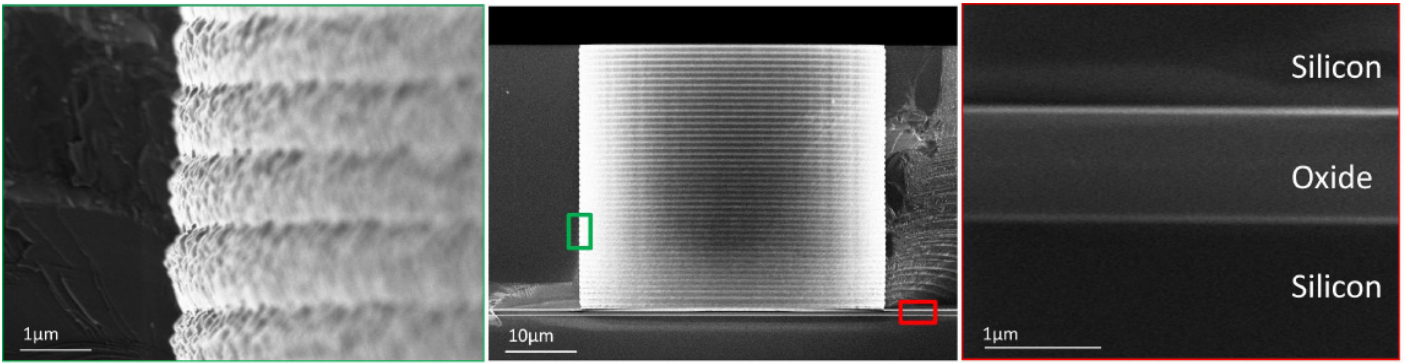
- Anodic bonding
- Direct bonding
- Eutectic bonding
- Glass frit bonding
- Adhesive bonding
- Metal thermo compression bonding

Technologies like anodic or direct bonding require high surface quality that will be realized using special CMP processes. Following the bonding process the wafer stack can be thinned to a specified final thickness

using grinding processes. Subsequently these wafers can be processed by its customers like original wafer substrates but already pre-structured and preconditioned. Fraunhofer ENAS offers wafers with either grinded or polished surfaces as well as electrical, mechanical, optical or fluidic structures as required. The specification of each semi-finished bonded substrates is determined in agreement with the customer, depending on the intended application.

## Equipment

- Mirra and IPEC 472 CMP tools
- Deposition by PVD, CVD, ECD
- Suss Cleaner CL 200
- Suss Bondaligner BA6/8
- Suss Substrate Bonders SB 6/8e
- EVG Aligner 6200 NT & Bonder 540
- STS Multiplex ICP
- Centrotherm High Temperature Horizontal Furnace
- Disco Dag 810
- SPS spin etch



## Material combinations

Fraunhofer ENAS offers different material combinations for MEMS applications, customer-specific solutions and special sizes up to 200 mm. The exact and technically feasible specification of each bonded substrate is determined in agreement with the customer.

### Overview about possible material combinations

	Silicon	Foturan glass	Borosilicate glass	LiTaO <sub>3</sub>	LTCC
Silicon	x	x	x	x	x
Foturan glass	x	x	x	x	
Borosilicate glass	x	x	x	x	
LiTaO <sub>3</sub>	x	x	x	x	
LTCC	x				

Figures:

page 1: Silicon-LiTaO<sub>3</sub>-Silicon wafer level stack including electrical redistribution

page 2: SOI-Wafer including through holes in 50 µm Si-devices

Photo acknowledgments:

Fraunhofer ENAS

All information contained in this datasheet is preliminary and subject to change. Furthermore, the described systems, materials and processes are not commercial products.